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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/750,190	12/30/2003	Carlos J. Gonzalez	SNDK.334US0	9150

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EXAMINER
LI, ZHUO H

ART UNIT	PAPER NUMBER
2185	

MAIL DATE	DELIVERY MODE
12/12/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

PTOL-90A (Rev. 04/07)

Office Action Summary	Application No.	Applicant(s)
	10/750,190	GONZALEZ ET AL.
	Examiner	Art Unit
	Zhuo H. Li	2185

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE <u>3</u> MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.
- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on <u>29 October 2007</u>.

2a)☐ This action is **FINAL.**   2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) <u>10,11 and 14-16</u> is/are pending in the application.

    4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) <u>10,11 and 14-16</u> is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

    Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

    Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

    a)☐ All   b)☐ Some * c)☐ None of:

      1.☐ Certified copies of the priority documents have been received.

      2.☐ Certified copies of the priority documents have been received in Application No. _____.

      3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

    * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1)☒ Notice of References Cited (PTO-892)

2)☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)

3)☒ Information Disclosure Statement(s) (PTO/SB/08)
    Paper No(s)/Mail Date <u>10/29/07</u>.

4)☐ Interview Summary (PTO-413)
    Paper No(s)/Mail Date. _____.

5)☐ Notice of Informal Patent Application

6)☐ Other: _____.

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1.   A request for continued examination under 37 CFR 1.114, including the fee set forth in

37 CFR 1.17(e), was filed in this application after final rejection. Since this application is

eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e)

has been timely paid, the finality of the previous Office action has been withdrawn pursuant to

37 CFR 1.114. Applicant's submission filed on 10/29/2007 has been entered.

Response to Amendment

2.   This Office action has been modified in response to the amendment filed 10/29/2007.

Information Disclosure Statement

3.   The information disclosure statement (IDS) submitted on 10/29/2007 was filed after the

mailing date of the final Office action on 6/20/2007. The submission is in compliance with the

provisions of 37 CFR 1.97. Accordingly, the information disclosure statement is being

considered by the examiner.

Claim Rejections - 35 USC § 103

4.   The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all

obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in
> section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are

such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

5.   Claims 10-11 and 14-16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Mukaida et al. (US Pub. 2003/0028704 hereinafter Mukaida) in view of Otake et al. (US 2004/0030825 hereinafter Otake).

Regarding claim 10, Mukaida discloses a flash memory system (1, figure 1) having an array of non-volatile memory cells (figure 2) arranged in blocks as a unit of erase, pages therein as a unit of data programming and reading and planes of plurality of blocks are independently accessible (figure 4 and page 6, [0105] to [0108]), a method of operation comprising logically forming metablocks, i.e., virtual block, that individually include a block from a plurality of the planes (2-0 through 2-3, figure 6, page 7 [0116] to [0120]), sequentially receiving write commands with varying amounts of data, i.e., series write command with successive host addresses, (page 9 [0164]), and variously writing all the data received with individual write commands (page 10 [0176]-[0178], i.e., sequential data write operation in response to the storage

of the external write command) sequentially into pages within individual blocks of one of the

planes (figure 12, and pages 10-11 [0180] to [0193]) (figure 22, page 17 [0289] to [0297], and

pages 20-20, [0345] to [0346]). Mukaida differs from the claimed invention in not specifically

teaching variously writing all the data in parallel into pages within two or more blocks of one of

the metablocks in two or more planes depending upon the amount of data received with the

individual host write command. However, Otake teaches a storing device controlling method

comprising the step of writing received data in parallel into pages within two or more blocks of

one of the metablocks in two or more planes depending upon the amount of data received with

the individual host write command (pages 2-3, [0036] to [0051], i.e., data for zm blocks are

written on m pieces of flash memories in parallel depending upon the size of data received with

individual host command), thereby improving the performance of writing in flash memories by

decreasing evacuation in rewriting (page 3, [0052]). Therefore, it would have been obvious to a

person of ordinary skill in the art at the time the invention was made to modify Mukaida in

having the step of variously writing the received data in parallel into pages within two or more

blocks of one of the metablocks in two or more planes depending upon the amount of data

received with the individual host write command, as per teaching of Otake, because it improves

the performance of writing in flash memories by decreasing evacuation in rewriting.

Regarding claim 11, Mukaida discloses the method further comprising writing an

indication into non-volatile memory cell (i.e., cell #2351-0, figure 20) at the same time as the

received data that identifies the blocks into which the data are being written in parallel (page 16,

[0275] to [0278]).

Regarding claim 14, Mukaida discloses a flash memory system (1, figure 1) having an

array of non-volatile memory cells (figure 2) arranged in blocks as a unit of erase, pages therein

as a unit of data programming and reading and planes of plurality of blocks are independently

accessible (figure 4 and page 6, [0105] to [0108]), a method of operation comprising logically

forming metablocks, i.e., virtual block, that individually include a block from a plurality of the

planes (2-0 through 2-3, figure 6, page 7 [0116] to [0120]), sequentially receiving write

commands with varying amounts of data, i.e., series write command with successive host

addresses, (page 9 [0164]), writing all the received data in parallel into individual pages of

individual blocks of only one of the sub-arrays in response to receiving the write commands with

a number of one or more sectors for only a signle page of data (figure 22, page 17 [0289] to

[0297] and pages 20-20, [0345] to [0346], i.e., data extending over a plurality of page can be

flash programmed simultaneously), and maintaining indications in the non-volatile memory cells

that are associated with the written sectors of data as to whether the individual sectors have been

written in logical sequence with other sectors in a single block (page 16, [0275] to [0278]).

Mukaida differs from the claimed invention in not specifically teaching the step of writing all the

received data in parallel into pages within a plurality of blocks of at least one of the metablocks

in a plurality of the sub-arrays in response to receiving the writing commands with a number of

sectors of data for a plurality of pages and maintaining indication that are associated with the

written sectors of data as to whether the individual sectors have been written in logical sequence

with other sectors of data received with the same write command as the individual sector in a

plurality of blocks of a metablock. However, Otake teaches a storing device control method for

writing the received data in parallel into pages within a plurality of blocks of the at least one of

the metablocks in a plurality of the sub-arrays (pages 2-3, [0036] to [0051] i.e., data for zm

blocks are written on m pieces of flash memories in parallel depending upon the size of data

received with individual host command) and maintaining indication that are associated with the

written sectors of data as to whether the individual sectors have been written in logical sequence

with other sectors in a plurality of blocks of a metablock (page 4, [0059] to [0064]). Therefore, it

would have been obvious to a person of ordinary skill in the art at the time the invention was

made to modify Mukaida in having the step of writing the received data in parallel into pages

within a plurality of blocks of the at least one of the metablocks in a plurality of the sub-arrays

and maintaining indication that are associated with the written sectors of data as to whether the

individual sectors have been written in logical sequence with other sectors in a plurality of

blocks of a metablock, as per teaching of Otake, because it improves the performance of writing

in flash memories by decreasing evacuation in rewriting.

Regarding claim 15, Mukaida teaches a table is stored within the non-volatile memory

cells and the sectors of data for a single page of data include data of the table (figure 25 and [age

18, [0308] to [0310]).

Regarding claim 16, Mukaida teaches to store the indications with their respective sectors

of data as part of header thereto ([0308]).

Response to Arguments

6.   Applicant's arguments filed 10/29/2007 have been fully considered but they are not

persuasive.

In response to applicant's argument that neither Mukaida nor Oake discloses executing write commands received by the flash memory system by either storing the data in parallel in multiple pages of a metablock extending across multiple memory planes or sequentially in blocks of a single plane, depending upon the amount data received with the write commands, it is noted that Mulaida teaches variously writing all the data received with individual write commands (page 10 [0176]-[0178], i.e., sequential data write operation in response to the storage of the external write command) sequentially into pages within individual blocks of one of the planes (figure 12, and pages 10-11 [0180] to [0193]) (figure 22, page 17 [0289] to [0297], and pages 20-20, [0345] to [0346]), and Otake teaches a storing device controlling method comprising the step of writing received data in parallel into pages within two or more blocks of one of the metablocks in two or more planes depending upon the amount of data received with the individual host write command (pages 2-3, [0036] to [0051], i.e., data for zm blocks are written on m pieces of flash memories in parallel depending upon the size of data received with individual host command). Thus one skill in the art would recognize the combination of Mukaida and Otake teaches the claimed limitations as recited in claim 10. In addition, the claimed language merely defined variously writing all the data received with individual write command in either first or second condition, such that any one of the condition as taught by the combination of Mukaida and Otake can read on the claimed limitations. Therefore, for these reasons, it is respectfully submitted that claim 10, and thus also its dependent claim 11, are rejected under the cited Mukaida and Otake references.

In response to applicant's argument on claims 14-16, it is noted that independent claim 14 is believed to be rejected for the same reasons given above for claim 10. Furthermore, Otake

teaches maintaining indication that are associated with the written sectors of data as to whether the individual sectors have been written in logical sequence with other sectors in a plurality of blocks of a metablock ([0060], parallelism degree field to show how many flash memories data being written). Thus, one skill in the art would recognize the combination of Mukaida and Otake teaching the claim limitations. Furthermore, Mukaida teaches a table is stored within the non-volatile memory cells and the sectors of data for a single page of data include data of the table (figure 25 and [0308] to [0310]). For these reasons, it is respectfully submitted that claim 14, and thus also its dependent claims 15 and 16, are rejected the cited Mukaida and Otake references

Conclusion

7.   Any inquiry concerning this communication or earlier communications from the examiner should be directed to Zhuo H. Li whose telephone number is 571-272-4183. The examiner can normally be reached on Tues - Fri 9:00am - 6:30pm and alternate Monday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Sanjiv Shah, can be reached on 571-272-4098. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

8.   Information regarding the status of an application may be obtained from the Patent

Application Information Retrieval (PAIR) system. Status information for published applications

may be obtained from either Private PAIR or Public PAIR. Status information for unpublished

applications is available through Private PAIR only. For more information about the PAIR

system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR

system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Zhuo H. Li
Patent Examiner

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